Analog-Signal Quality Characterization of the FLITES Distributed 192-Channel Data Acquisition System

Analog-Signal Quality Characterization of the FLITES Distributed 192-Channel Data Acquisition System

E. Fisher[1], Y. Yang[1*], S-A. Tsekenis[1], N. Polydorides[1*], C. Liu[1], H. McCann[1] and P. Wright[2]

[1] School of Engineering, Institute for Digital Communications, University of Edinburgh (Edinburgh, UK)
[2] School of Electrical and Electronic Engineering, University of Manchester (Manchester, UK)

[*]Email: y.yang@ed.ac.uk or n.polydorides@ed.ac.uk

ABSTRACT

The Fibre-Laser Imaging of gas Turbine Exhaust Species (FLITES) project continues to target chemical species tomography for quantification and video-rate imaging of Carbon Dioxide within the exhaust plumes of high-thrust aero-jet engines. This remit, and the scalability needed to i) increase imaging speeds and resolutions and ii) extend it towards other pertinent gases, have been iteratively tackled through custom mechanical, optical and electronic designs targeting a commercial engine testing facility. We previously published work towards a high-speed (40MS/s/channel 14-bit) and multi-channel (192-input) fully-parallel data acquisition (DAQ) system, utilizing Ethernet connectivity for remote operation and field-programmable gate array (FPGA)-based digital lock-in amplification (DLIA). The data rates are significant, 8.96Gb/s for a single printed circuit board (PCB) and over 107.5Gb/s for the 12-node, full-system. The management of sixteen (560Mb/s) low-voltage differential-signalling (LVDS) dual-data-rate (DDR) lines per FPGA has presented significant challenges, which we discuss here in overview. However, for the accurate analysis of gas concentrations, using tunable diode-laser absorption-spectroscopy (TDLAS) and wavelength-modulation spectroscopy (WMS), the analog performance is of interest and will be discussed. Specifically, while a 1st order 10Hz high-pass and 2nd order 3MHz low-pass response have been previously confirmed, we achieve a best-case signal-to-noise ratio (SNR) of 55.76dB, a spurious-free dynamic range (SFDR) of 50.8dB and a thermal noise floor of -60dB. The inputs are shown to be linear over the range of 0-1600mV (2Vpp ADC range) and the limiting factor is found to be harmonic distortion induced by single-sample glitches that are possibly linked to high-frequency simultaneous switching noise.

Keywords Data Acquisition, Chemical Species Tomography, Tunable Diode Laser Absorption Spectroscopy, Distributed Signal-Processing

Industrial Application Aerospace and Aviation, Emissions Monitoring

1 INTRODUCTION

The FLITES project seeks to tomographically image the pollutant gas species present in the exhaust plumes of high-thrust, high-bypass commercial aero-jet engines. The central motivation for such a project is to address the instrumentation needs of the aviation sector to better enable development of high-efficiency engines, optimised combustion, bio-fuel mixture development and the overall reduction in pollutants to meet the ever-stringent emissions legislation of the sector (ATAG, 2015). The FLITES project has developed a 126-beam tomographic setup, which is now installed within a Rolls-Royce testing facility at Instituto Nacional de Técnica Aerospacial (INTA, Madrid). This spectrographically targets an absorption feature of Carbon Dioxide (CO_2) (Bolshov, 2015), (Rieker, 2009), (Wilson, 2014), however through modification of key parameters and sub-systems the instrument is intended to scale to other gas species such as water vapour (H_2O), unburnt-hydrocarbons (UHC) and the oxides of Nitrogen (NO_x). Further, recent advances in chemical species tomography (CST) present the idea of obtaining the temperature profile of the exhaust plume (Ma, 2013), and by obtaining high-frame rate images (100 fps) the dynamics of gas mixing within the plume (Harley, 2012) can complement existing rake (intrusive) testing and computational fluid dynamics (CFD) simulation. Scalability has been directly addressed in this instrument, where basic concepts – such as unique addresses for Ethernet connected data acquisition (DAQ) hubs – allows the number of beams to be quickly increased (Fisher, 2016). Likewise, a specification push ensuring design for adaptability – such as real-time modification

of operating variables and settings – allows the instrument to sweep parameters or adapt its measurement methodology for particular experiments (Fisher, 2016).

By way of an overview of this project's systems, a 7 m dodecagonal mounting ring has been designed, which holds custom kinematic launch and receive optics upon alignment plates that guarantee a planar and perfectly parallel tomographic imaging plane (Wright, 2016). This is mounted 4 m behind Rolls-Royce jet-engines such as the Trent 1000 and the Trent XWB. At present 126 beams are installed, with a regular (21-beam, 6-projection) tomographic sinogram designed to obtain approx. 10 cm resolution within a 1.8 m central area suitable for estimated plume diameters of 1.4-1.6 m (Tsekenis, 2016). The first iteration of this instrument targets a CO_2 absorption feature at 1997 nm using both tunable diode laser absorption spectroscopy (TDLAS) and wavelength modulation spectroscopy (WMS) obtaining the path concentration integral (PCI) of the gas for each pencil beam (Wilson, 2014), (Fisher, 2016), (Wright, 2016), (Tsekenis, 2016). Significant work has been done (Rieker, 2009) to remove calibration steps within the gas sensing techniques, culminating in the use of a fundamental (1f) and second harmonic (2f) normalisation approach (Fisher, 2016), (Wright, 2016), (Tsekenis, 2016). To reduce costs and system complexity, the amplitude- and wavelength- modulated narrow line-width laser beams for this system are provided by a single TDLAS/WMS modulated seed laser, which is then passed to each of the 126 launch elements via a 1.5-2.0-Watt Thulium-doped fibre amplifier (TDFA) and a fibre network consisting of splitters with ratios 1:6 and 1:21 (Wright, 2016), (Tsekenis, 2016). To capture this light after it has passed through the plume, the receiver elements use extended InGaAs photodiodes with at-site differential transimpedance amplification and high drive-strength output buffering (Fisher, 2016). To date, this system has been proven by gaseous phantom tests closely replicating the expected CO_2 concentrations and air temperatures (Tsekenis, 2016), while tomographic reconstruction methods based upon constraining the reconstructed values to be zero or positive have also been developed (Polydorides, 2018). The system installed at INTA in late 2016, uses a 16-way time-multiplexed (128 to 8) National Instruments data acquisition system which is sufficient for 3 fps tomographic imaging, however this must perform initial digital signal processing (DSP), spectrographic analysis (Benoy, 2016) and tomographic reconstruction (Wright, 2016), (Tsekenis, 2016), (Polydorides, 2018) offline within the Matlab environment.

A significant proportion of the work done by The University of Edinburgh, supported by academic collaborators at Strathclyde and Manchester, within this project has been the development of a custom data acquisition system (Fisher, 2016), (Fisher, 2018). This is intended to push the imaging rate towards 100 fps, provide fully-synchronous multi-channel acquisitions suitable for the high (150-200 m/s) gas flow velocities that are expected and allow expansion towards embedded real-time 2f by 1f normalisation. To this end, we have presented the prototype design for a 12-node, 16-channel per node DAQ with a total of 192 40 MS/s 14-bit analog channels with 10 Hz 1^{st} order high-pass and 3 MHz 2^{nd} order low-pass frequency responses (Fisher, 2016). The TDLAS coarse wavelength modulation ramp rate is designed to be within the range of 1 Hz to 100 Hz, while the fine wavelength dither for WMS is designed to be within the range of 100 kHz to 500kHz (1MHz second harmonic). To significantly increase measurement signal-to-noise ratios (SNRs) in the presence of noise terms such as the exhaust plume's refractive index beam distortion/wander and electrical or vibrational noise, along with reducing the high data rates expected (8.96 Gb/s per hub and 107.5 Gb/s total), an on-ring, distributed digital lock-in amplification (DLIA) (Chighine, 2015), (Lascos, 2008), (Ayat, 2016) strategy is also utilised. This paper will discuss characterization of captured real-world analog signals along with the strategies, sub-system designs and the significant challenges of high-speed fully-parallel custom data acquisition systems.

2 FLITES DATA ACQUISITION – AN OVERVIEW

Before discussing the DAQ designed within the FLITES project (Section 2.2) (Fisher, 2016), (Wright, 2016), (Tsekenis, 2016), (Polydorides, 2018), (Fisher, 2018), it is prudent to discuss the specifications and alternative instrumentation methods suitable for an academic project, operating at large scales, hosted within commercially-important, harsh-environment industrial testing facilities.

2.1 Specifications and Commercial Hosting Requirements

Firstly, the intended test cell requires a minimum cabling distance of 50 m from the test cell's gantry to the control room (no human operators can be within the cell during tests). Coupled with the half-

circumference of the tomographic mounting ring (11 m) and the number of beams (126) approx. 7,700 m of cabling would be required to pass analog signals from photodiodes within the receiver elements to the control room. Naturally, this is not feasible because of: i) the cost and practicalities of such extensive cabling, ii) the drive strength needed by on-ring circuitry and iii) noise pick-up concerns or shielding. Likewise, at the control room, high-speed 126-channel data acquisition would still be needed. Therefore, a hierarchical data acquisition approach has been taken whereby photodiode pre-amplifiers can be placed within the receiver elements and 12 digitization 'hubs' can be placed on the ring itself (Fisher, 2016), (Wright, 2016), (Tsekenis, 2016). This significantly reduces cabling, allowing a maximum of 2.5 m between photodiode pre-amplifier and a corresponding analog-to-digital converter (ADC). Likewise, it allows the signals to be digitized and processed at-site, affording both i) the advantages of high-bandwidth digital back-end networking (Fisher, 2018) for scalability etc and ii) significantly lower noise than would be expected in a fully-analog 60-70 m per channel architecture.

Secondly, the environment into which this system is deployed is both a high-vibration and dirty environment (Wright, 2016). It is fully expected that during tests, water, oil, soot and fuel will all be present in large quantities at the imaging plane. As a further requirement, the testing cell is a working commercial engine facility requiring ruggedized systems and assurances that the equipment will not interfere with either engine diagnostic instrumentation or the air flow dynamics within the cell itself. Our base specifications for this data acquisition system are:

i) Real-world unprocessed data noise figures of 50dB with focus on harmonic noise,
ii) A yield from 192 channels, (including some redundancy), for at least 126 channels (66%),
iii) A sample rate offering a factor of 5-10 processing gain above Nyquist (10-20MS/s),
iv) Fully-differential analog inputs with at least 2Vpp and 14-bit digitization, which is flat over frequency (100 Hz to 1 MHz) and linear over amplitude,
v) A real-time processing block able to obtain in-phase (I) and quadrature (Q), first (1f) and second (2f) harmonic lock-in amplification of at least 126 simultaneous channels with software control of: a) the DLIA time constant, b) the reference frequency and c) phase,
vi) Per-node (12) synchronisation to the central seed-laser driver offering at least 400 DLIA points per TDLAS scan, adaptable ramp and wavelength dither between 1 and 100 ramps/s and 100 and 500 kHz respectively with sub-dither period synchronisation across the ring (better than 1us),
vii) Capacity for an output rate of over 400 DLIA samples (32-bit) with I, Q for both 1f and 2f (4-words) from 12 channels per node (min) at an imaging rate of 100 fps (59Mb/s), and
viii) Software control including, start, stop, resets, enables and unique node addresses.

2.2 Architecture Choices and DAQ Figure of Merit

While all instrumentation projects must choose between a commercial off-the-shelf (COTS) or application-specific bespoke solution, it was felt that future real-time imaging capacity could be best addressed though a custom DAQ design (Fisher, 2016), (Wright, 2016), (Tsekenis, 2016). This has partly been necessitated by the specifics of the photodiode preamplifiers (differential) (Wright, 2016), (Tsekenis, 2016), the need of including at-site real-time DLIAs, the requirements of the TDLAS/WMS gas-concentration spectroscopy (Bolshov, 2015), (Rieker, 2009), (Wilson, 2014), (Benoy, 2016) and costs per channel. However, during the years since the project's proposal, companies can offer ruggedized, Ethernet connected, parallel, multi-channel DAQ systems. These now provide advantages with respect to the development time needed to obtain scientific data especially when their cost is normalized by sampling rates, noise performance, back-end functionality and embedded signal processing provisions and when combined with some lower-complexity analog multiplexing. For feasibility, the figure of merit in Eqn 1 can be used, where: C is the total cost of the system (excluding VAT), N_{chan} is the number of channels, SNR is the typical signal-to-noise ratio obtainable on a channel (dB), R_s is the sampling rate (MS/s) and R_d is the maximum back-end data throughput (Gb/s). This is an extension of the classic cost per channel metric, the point being to minimise the FOM by achieving a low cost per channel with high analog bandwidth and measurement accuracy alongside sufficient bandwidth to output unprocessed data. One could also normalise this FOM based upon i) available memory within a DAQ as this may be crucial for the capture of long-term, continuous data or ii) the embedded fixed or floating-point operations per second as a measure of real-time signal processing capabilities. The cost of labour and a robust estimate of required development man-years is also needed to adequately normalise this FOM to aid the comparison between academic vs industrial development of such a system.

$$FOM = \frac{C}{N_{chan}} . \frac{1}{SNR} . \frac{1}{R_s} . \frac{1}{R_d} \quad (1)$$

2.3 FLITES DAQ System Overview

The design of the FLITES data acquisition system is well covered in (Wilson, 2014), (Fisher, 2016), (Wright, 2016), (Tsekenis, 2016), (Polydorides, 2018), (Fisher, 2018), (Chighine, 2015), however as an overview, each DAQ hub supports 16 fully-differential analog inputs, which pass to two octal ADC integrated circuits (ICs), in this case Analog Devices AD9257. These ADCs offer a low system level cost in comparison to a bank of 16 single ADCs due to the use of shared packages, IO pins and common resources on the silicon (reference voltage, configuration, clock dividers, setup logic etc). Both ADC packages (left and right) are clocked at 160MHz from a phase-locked loop (PLL) IC at the centre of the PCB (Fig. 1). The 14-bit data is passed to a central field-programmable gate array (FPGA), Xilinx Spartan 6 LX45 using a source synchronous approach (Xilinx, 2018) whereby both a data clock (DCO = 280MHz) and framing signal with deterministic data pattern are provided. The FPGA therefore has twenty high-speed low-voltage differential signalling (LVDS), dual data rate (DDR) traces as its primary inputs. The difficulty here is that along with these, FPGA IO is also required for interfacing to the a) 100BASE-TX Physical layer Ethernet IC, b) 256Mb SDRAM, c) 256Mb FLASH, d) 16Mb PROM, along with the peripheral interfaces such as JTAG, UART, SPI (x2), I2C and a set of headers for debug and future expansion. The PCB also includes a 3-axis accelerometer and a 14-bit temperature sensor for diagnostics and variable threshold coaxial input ports for the synchronisation of the system using the ramp and dither signals from the TDLAS/WMS laser controller (Fisher, 2016), (Wright, 2016), (Tsekenis, 2016).

While each PCB can be assigned a unique address using its medium access controller (MAC) or internet protocol (IP) address in the embedded C software, functionality is included on the PCB for a switch-based assignment of address, currently with 2^4 addresses. When complemented with unused expansion header pins or future PCB re-spins, the address space can be easily expanded, while the current system installed on the ring uses a maximum of eleven of the sixteen channels per PCB allowing significant expansion and redundancy per PCB. The FPGA was selected based upon the available component budget, an initial estimate of four Xilinx DSP48A1 slices per DLIA (Bolshov, 2015) (Rieker, 2009), (Wilson, 2014) and the known number of independent ADC channels for total FPGA IO budgeting. The developed PCB is a first-round prototype, allowing significant scope for a fast turn-around of subsequent, higher-specification DAQ Hubs. For example, if needed, the ADCs are footprint compatible with a 65 MS/s per channel version, while the FPGA can be upgraded from the LX45 to the LX75 (171% increase in logic slices and 229% increase in DSP slices) and the Ethernet PHY can be upgraded from 100Mb/s to 1000Mb/s. Despite this scope to expand the digital sub-system, we expect that a second or third generation DAQ design would prioritize low-noise analog functionality with a) a noise floor better than 65 dB, b) scope for programmable gain (e.g. x0.25, x0.5, x1, x2, x4), c) optimised noise bandwidth for the TDLAS/WMS methodology and d) significant attention to signal integrity, cross-talk and harmonic noise mitigation.

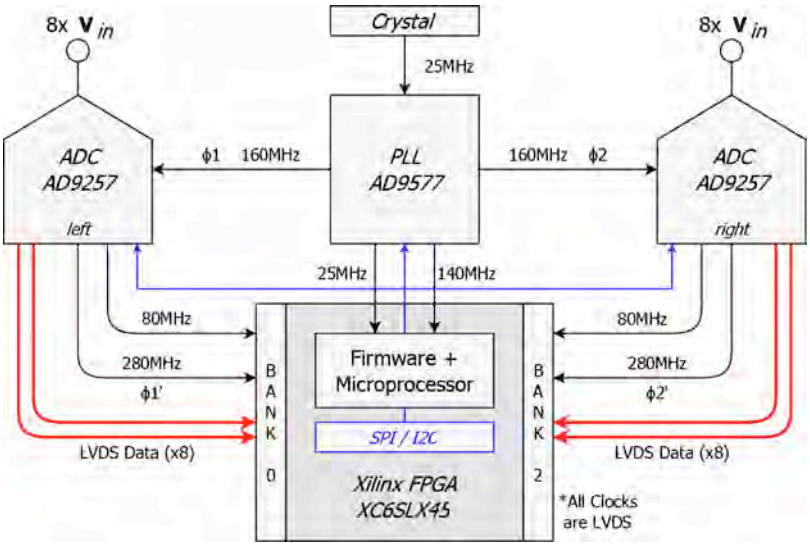

Fig.1. The clocking and data transfer architecture for 16 independent 40MS/s 14-bit ADC channels to a central Xilinx field programable gate array on the FLITES DAQ Hubs. All clocks and data are LVDS, while the data is in dual data rate (DDR) format. The PCB's PLL and ADCs are configured upon bootup via I2C and SPI interfaces respectively and allow parameters such as sampling rate to be modified from the software level.

3 HIGH-SPEED LVDS INTERACES – DESIGN AND CHALLENGES

In this system, the 40MS/s 14-bit ADCs provide data at 560Mb/s per channel. This leads to a data eye or unit interval (UI) of 1.785 ns and from a rise/fall time of 350 ps a trace knee-frequency of 1.43 GHz. However, to ensure that this data is received with a bit error rate (BER) better than $0.17x10^{-6}$, and a sample error rate (SER) of $2.5x10^{-6}$, i.e. approx. one erroneous bit per TDLAS ramp ($5.6x10^{6}$ bits), several factors need to be considered. In this section, a short overview of the design and challenges experienced will be discussed to aid others wishing to design similar systems (Xilinx, 2018).

3.1 PCB Design Considerations

Firstly, as the data uses low-voltage differential signalling (LVDS), the timing of the differential traces needs to be well matched, in this case the PCB differential traces are length matched to within 750 µm. This reduces the prospect of one trace of the differential pair transitioning before the other, which would a) reduce the skew margin within the already time-constrained data eye and b) would dissipate extra power as both arms of the receiver's current-steering differential pair would be active for this short period.

Differential traces act as their own high-speed current returns, however we use a solid ground plane in the PCB layer stack as a firm reference plane. Power planes within the PCB are necessarily split into power regions, however this should have minimal impact on the differential trace characteristic impedance, which will be dominated by trace width and spacing requirements. The traces are designed for a 100 Ohm characteristic differential-impedance which is matched at the FPGA receiver using the "DIFF_TERM" IO directive to add an internal 100 Ohm termination resistance. The LVDS standard is more accurately thought of as a current-mode transmission using current-steering of 3.5 mA. When dropped across the termination resistance, this leads to a 350 mV voltage swing and significant immunity to common-mode noise sources. Despite this, signal integrity can still be an issue.

Between the data and clock lines, length matching can be relaxed to aid the layout and cost. Here, the traces are matched to within 3 mm as PCB area can be quickly exhausted when implementing serpentine length tuning. To account for PCB routing delays between data and clock lines, the Xilinx IO delay resources (Xilinx, 2018) can be added per channel allowing tunable delays in 16-20 ps increments. While PCB trace delays can be minimal, ensuring all traces are either longer or shorter than the clock will aid timing closure, removing the need for a mixture of positive and negative delays. In many delay scenarios negative delays are implemented by a delay greater than the data UI, which, while still able to position the sampling point within the centre of the eye, yields a one-bit timing offset.

3.2 Logic Design Considerations

Rather than using FPGA fabric-level flip-flops with lengthy setup and hold times (470 ps and 390 ps respectively for Xilinx Spartan 6 LX45 at speed grade -2), the dedicated ISERDES2 resources can be used to capture and decode the ADC data with setup and hold times of (240 ps each). This allows a timing headroom budget to be created that allows assessment as to design margins for both: a) PCB trace data-clock skew and b) internal FPGA clock skew. An example timing closure analysis is shown in Table 1, where care must be taken with the total clock skew internal to the FPGA. As this includes the routing of the data clock over multiple clock regions within the FPGA IO bank and the clock must pass through several buffers prior to use, the timing becomes more complex as a result. Note that this analysis considers an ideal signal integrity scenario, however to account for a more realistic condition, a timing margin of 100 ps can be included.

To perform multi-channel data acquisition, multiple IO banks and multiple clock regions within these banks must be used. This complicates the clocking architecture significantly as we must bridge an entire IO bank with a single data clock, while also respecting that clock regions have separate clocking resources (buffers etc) with different on-FPGA delays. This system uses a 560 MHz dual-data-rate clock, a 280 MHz single-data-rate clock (from the ADC), an 80 MHz 7-bit nibble clock (DIV_CLK) and a 40 MHz 14-bit word clock. This latter clock is used for all signal processing logic (DLIA and DDS) associated with the input SerDes of a specific bank (see Fig 2), i.e. the left-hand side ADC goes to Bank 0, while the right ADC goes to Bank 2.

Table.1. Timing budget for a 560 Mb/s LVDS DDR serial data link. To meet timing closure the total delays on the serial data sampling clock internal to the FPGA must be well matched to the FPGA input data delays.

Timing Parameter Value:	Value (Pico-Seconds):	Notes:
Total	1785	*Assuming 40 MS/s 14-bit*
Rise Time within Eye	175	*ADC output 10-90%*
Fall Time within Eye	175	*ADC output 10-90%*
Differential _P/_N Skew Margin	10	*Differential length matching*
SerDes Input FF Setup Time	240	*From Xilinx xapp1064 page 22*
SerDes Input FF Hold Time	240	*From Xilinx xapp1064 page 22*
Total of all Jitter Processes	50	*160MHz clock jitter + ADC data clock jitter + PCB trace induced jitter + FPGA internal bit, nibble and word clock jitter*
Remaining Time within Eye	895	*[50.1% of UI] Without PCB trace data skew or FPGA internal clock buffer, divider, routing skew*
PCB Trace Skew	Must be < 100	*3mm data-clock matching gives approx. 20-30 ps*
FPGA Clock Skew	Must be < 800	*Data clock buffer delay + data clock routing delay + DDR clock creation delay*

The decoding of the 14-bit data represents an issue as only deserialization ratios of one to eight are supported by the Xilinx Spartan 6 FPGA family. To de-serialise the 14-bit data, we first perform deserialization with a SERDES ratio of 7, creating upper and lower nibbles. This data is then word-synchronously combined and decimated to 40 MHz 14-bit.

As with all FPGA designs, (in comparison to CMOS IC designs), the focus is on logic and not IO or clocking reconfigurability, consequently for multi-channel high-speed IO the clock resources represent a portion of the design where user reconfigurability is of lower priority than low-jitter, low-skew, optimised placement and routing. In this particular case, this manifests itself as an increase of complexity with respect to the nibble-level clock (80 MHz) generated by clock dividers operating at the SerDes ratio (=7). While the static timing analysis tools have full knowledge of input and logic usage timing and physical constraints, and the delays associated with the buffers and routing of all signals, the clock dividers themselves do not include clock enable lines, resets or methods of synchronising their internal dividers. As such, for a single IO bank (servicing 8 channels), there are two 80 MHz (nibble) and two 40 MHz (14-bit word) clock domains. Clock domain crossing setup and hold timing closure can be arranged through design, however the two DIV_CLKs represent an issue when it comes to bit-slip framing lock as a frame lock between the ADC and one of the DIV_CLK domains does not guarantee frame locking to the other, unsynchronised DIV_CLK domain. To alleviate this

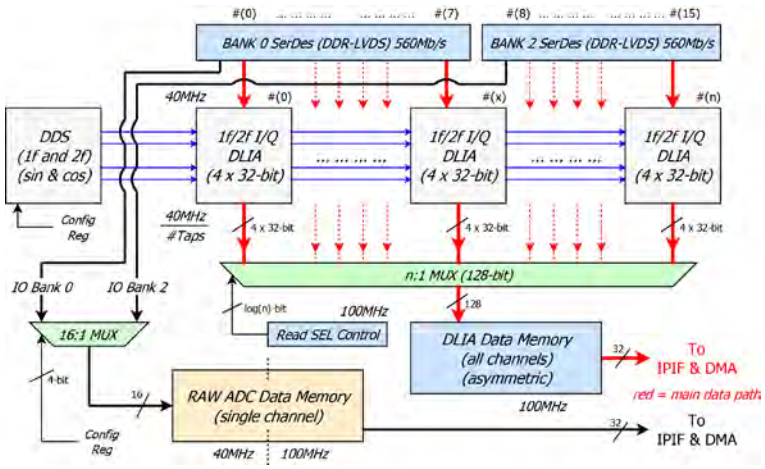

Fig.2. The high-speed serial data interfaces and the front-end digital signal processing implemented using Verilog hardware description language (HDL) within the FPGA. The 4-word 32-bit per word data from the digital lock-in amplifier blocks is sent to a large first-in-first-out (FIFO) memory block, while a software configurable channel multiplexer allows a single-channel to be piped to a 960-sample FIFO for laser and channel diagnostics. Both FIFOs are grabbed via an embedded microprocessor direct-memory-access (DMA) engine and custom intellectual property interfaces (IPIF).

issue, the fully-working bit-slip control state machine methodology is currently being expanded to include a higher-level state machine that periodically switches the frame locking feedback loop between these two domains to ensure both 80 MHz DIV_CLK regions are frame locked to the ADC's dedicated framing signal.

3.3 SerDes Interface Challenges and Issues

Normally with complex Silicon IC or FPGA designs, two methods are used to ensure design robustness and minimal data glitches. Firstly, register-transfer-level (RTL) formal verification and timing closure can be used as part of the universal design methodology (UDM), however this becomes complicated when dealing with high-speed interfaces to external components as a full mixed-signal model is required for the input data stream (including delay, jitter and clock skew) and often requires timing parameters that can only be estimated, e.g. PCB track delays or the magnitudes of signal integrity reflection coefficients. Secondly, loop-back testing using deterministic data fed into specific nets between functional blocks can be used during the debug cycle, for example before and after a signal processing block and as input to a FIFO. This latter technique is suitable for FPGA design, complementing timing sign-off within the logic synthesis tools, however the use of this technique for ADC interfaces relies on the availability of deterministic testing and framing patterns from the ADC itself (industry standard for high data-rate serial output ADCs). While these patterns aim to test a wide portion of the 2^{14} bit-space and can target different fundamental frequencies, many high-speed links require feed-back loop based data and frame locking techniques to be implemented at the receiver.

For this application with sixteen independent high-speed inputs, the issue is correct 14-bit data framing given the: i) non-deterministic ADC turn-on to first ADC output bit and b) first decoded 14-bit word delay relative to the FPGA's internal word-level clock. As standard, bit-slipping (Xilinx, 2018) can be used with a controlling state machine operating on the ADC's deterministic framing pattern. However, this does not consider channel to channel variations in timing or signal integrity and culminates in a complex interaction between the bit-level and word/nibble levels of the serial input hierarchy.

4 ANALOG CHANNEL CHARACTERISATION

The first tests conducted on the full analog channels were checks as to the digitisation of pure sinusoidal waveforms delivered from a 70 dB SNR arbitrary waveform signal generator. In figure 3, the correct sinusoid is shown with a good SNR and SFDR (left). However, as per the section above regarding the complexities of high-speed serial data transfer, figure 3 also shows a waveform of similar properties with significant distortion of the sinusoidal wave (right). This has been shown to be a result of an incorrect data frame alignment despite the system locking to the ADC's framing signal.

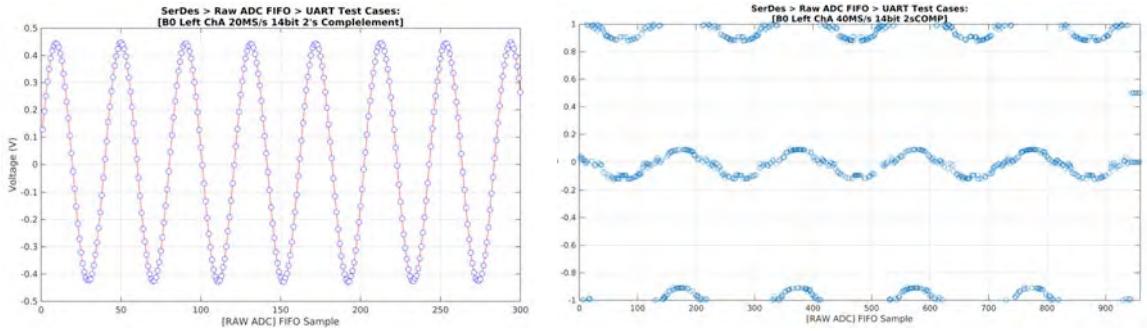

Fig.3. Left) a correct data transfer between ADC and FPGA with full frame locking and minimal sampling issues within the data eye (signal generator at 1000mVac-pp), and Right) an early erroneous transfer (signal generator at 200mV ac-pp) showing an issue with the most significant bit (MSB), which in this case is the signing bit of the two's complement format, leading to the sinusoid erroneously crossing the zero line.

In figure 4, the linearity of a single channel (B2-L-CC, Channel 14) has been tested with a 200 kHz single-tone sinusoid (40 MS/s mode) over the design input peak-to-peak amplitude range, with two tests per input amplitude. While the ADCs have an input range of 2000 mVpp the channel becomes slightly nonlinear as the amplitude is increased past 1750 mVpp. This is expected to be due to the lower headroom available between the AC signal and the power supplies once the non-central DC bias point is taken into account. The figure also shows the measured typical and the upper and lower constraints of the channel gain as obtained by gain non-uniformity tests on multiple channels. In red, a

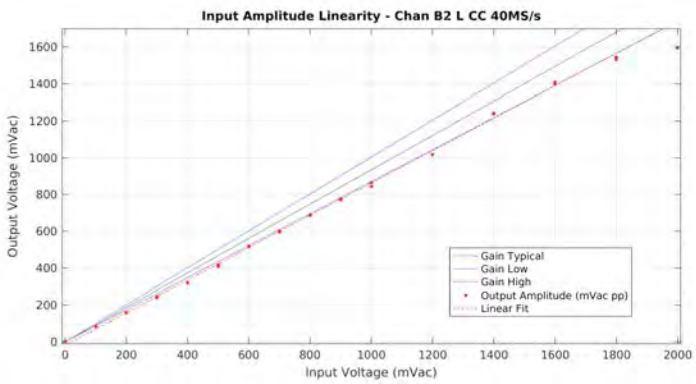

Fig.4. Analog input linearity over the range of 0mVac to 2000mVac peak-to-peak, as measured using a single sinusoidal tone at 200kHz using 14-bit 40MS/s mode. Also shown are i) the measured typical, minimum and maximum analog chain gains over multiple channels and ii) a linear fitting to the measured linearity data agreeing with measured channel gains

linear fit to the data from 0 mVpp to 1600 mVpp is shown to exactly match the lower extent of the variability between channels. Each point represents the measured amplitude obtained from at least 4 periods of the sinusoid within a 960-sample acquisition. Pre-manufacture simulation showed a channel gain of -0.7 dB, while the measured multi-channel median gain was -0.59 dB (i.e. a factor of 0.93). In figure 5, a high-performance channel is analysed for its run-to-run variability at 20 MS/s with a 500 kHz sinusoid at 1000 mVpp. Acquisitions were spaced by approx. 1 minute while a full system power off-on cycle was performed after run #17. While the SNR seems to be independent of this power cycle, the SFDR appears to improve over time between run #1 and run #17 and returns to its initial 44-45 dB level post power cycling. We note a maximum SNR of 56.5 dB, limited by harmonic noise, and a maximum SFDR of 50.79 dB, prior to the SNR improvement action of later DLIA processing. To look at the thermal noise floor, a test was performed whereby the signal generator is set to force a firm 0 mVac-pp 0 mVdc 0 Hz condition at the 200 Ohm termination resistor at the start of the analog signal chain on the Hub boards. This was performed on a channel exhibiting no data glitches in its serial data link, with correct frame locking. This is shown on the left of figure 6, where the majority of the noise is between 1.50 mV and 4.0 mV, giving an RMS of 3.2 mVdc and a noise amplitude of approx. 3 mVac. This equates to a thermal noise floor of approx. 56.5 dB. The reliability of two high-performance analog channels has also been tested over the course of approximately 2 hours (Fig 7). This early reliability analysis shows no loss of framing-lock and no detrimental noise or malfunction within this period. This is partially verified by bit-error rate analysis of the MSB and LSB of the de-serialised framing signal, which showed that once frame-locking is achieved, it is able to retain lock for significant periods, i.e. a framing signal BER better than $1x10^{-12}$.

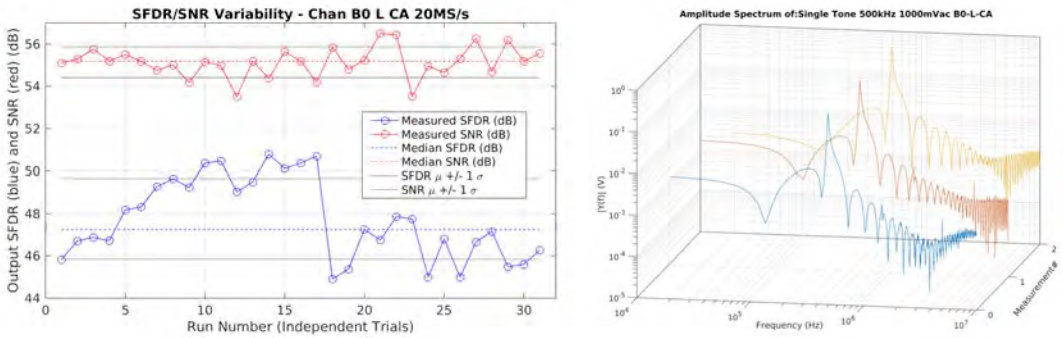

Fig.5. Left) SFDR and SNR multiple run variability for a high-performance channel. Also shown are the median and mean +/1 one standard deviations. At present, the mechanism causing this variability in performance has not been identified, and Right) the fast Fourier transforms (FFTs) of three independent measurements from channel B0-L-CA with a single-tone input of 500 kHz, 1000 mVac-pp. All raw acquisitions are obtained by the RAW FIFO in Fig 2 and are captured via UART.

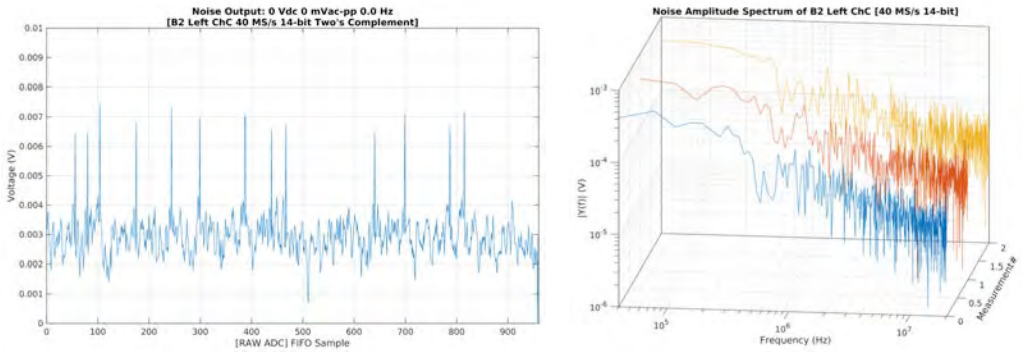

Fig.6. Left) a recorded time-trace of input noise for the channel B2-L-CC at 40 MS/s, and Right) the FFTs of three independent measurements, (same channel, same conditions).

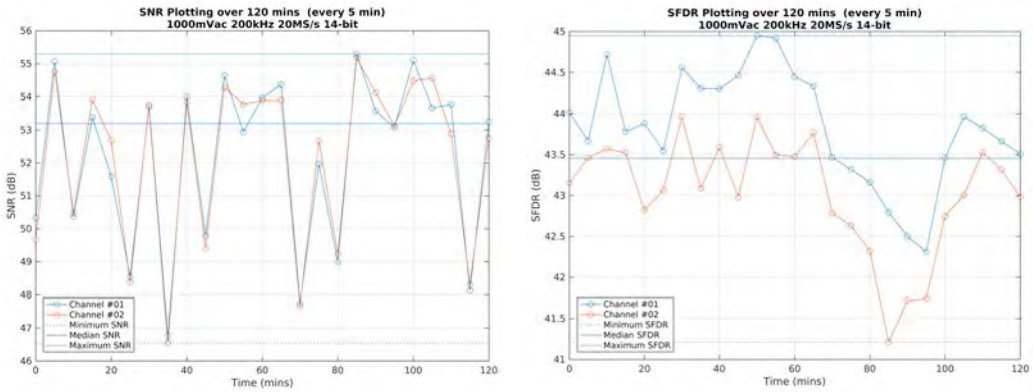

Fig.7. Long-term (2 hours) tests of Left) the SNR, and Right) the SFDR for two channels. The input was a 1000 mVac-pp 200 kHz sinusoid. Each point is taken every 5 minutes and is formed of a 1000 sample acquisition at 20 MS/s.

5 CONCLUSIONS AND FUTURE WORK:

In this paper the progress towards a 192-chan parallel, distributed, high-speed data acquisition system has been presented. While analog characterisation shows that the system is able to obtain the correct design bandwidth (10 Hz to 3 MHz), correct analog sampling (40 MS/s at 14-bit), is linear (0 mVac to 1600 mVac) and has mid-range noise (55.76 dB SNR) and harmonic distortion figures (50.8 dB SFDR), the design process has been lengthened due to the complexity of the high-speed data links.

These low-voltage differential, dual data rate links between the sixteen ADCs per DAQ Hub and the FPGA placed on each PCB, represent three areas where careful design and an increase in complexity are required. Firstly, PCB trace lengths must be impedance and length matched. Secondly, high-speed clocking of the serial data must use the dedicated resources offered by companies such as Xilinx or Intel (Altera). We note that fabric level flip-flops have insufficiently short setup and hold periods for the static timing budget of a 1.78 ns (560 Mb/s) data eye or for prospective high-sample-rate (65 MS/s) ADCs with timing budgets of 1.1 ns (910 Mb/s). While clock-to-data delay tuning can be used to remove static delays introduced by PCB trace differences, most designs above data rates of 650 Mb/s will need to use dynamic rather than static capture to optimally place the sampling point within the serial data eye. Thirdly, framing of the serial data represents a complex issue, even at the modest data rates used in this project. Bit-slipping and frame locking to the ADC frame signal is a good first approximation, however as PCB and FPGA data and clock delays or jitter sources can easily be cumulatively larger than the data eye, locking to the framing signal does not guarantee data frame lock on independent channels. In this design, the multiple clock domains in the FPGA IO banks have presented issues requiring an increase in complexity, however we note that for higher speeds or increased robustness, periodic training sequences using deterministic data is a preferred method and is widely used in combination with dynamic capture of Gb/s wireline links.

There are two themes to this FLITES DAQ work moving forward into 2019 and the recently funded CleanSky2 proposal. The first is to apply the above DAQ Hubs to gas cell tests of CO_2 verifying the

time and frequency response is suitable for TDLAS/WMS. In part, this has already been verified through early time-domain tests of the DLIA architecture and recent bit-level verification of the re-developed DLIA hardware description language (HDL) FPGA-code. The second theme is to install this hardware onto the tomographic ring currently hosted at the INTA testing facility (Madrid, Spain). This latter theme is to be run after the current installed 128-way time-multiplexed data acquisition system has been able to get slow-rate (approx. 3 fps) imaging of CO_2 concentrations of the jet-engine exhaust plume. Longer-term, future work will a) increase the technology readiness level (TRL) of the entire FLITES tomographic system and will b) start to expand the gas sensing methods to species such as water vapour, carbon monoxide, unburnt hydrocarbons and the oxides of nitrogen and sulphur.

REFERENCES:

AIR TRANSPORT ACTION GROUP (ATAG), (2015), Climate Action Takes Flight: The Aviation Sector's Climate Action Framework, White Paper, November 2015, Geneva Switzerland, URL: http://www.atag.org/component/downloads/downloads/311.html

AYAT, M., KARAMI, M., MIRZAKUCHAKI, S. and BEHESHIT-SHIRAZI, A., (2016), Design of Multiple Modulated Frequency Lock-In Amplifier for Tapping-Mode Atomic Force Microscopy Systems. IEEE Trans. Instrumentation and Measurement (TIM), Vol 65, No 10, 2016

BENOY, T., LENGDEN, M., STEWART, G. and JOHNSTONE, W., (2016), Recovery of Absorption Line Shapes with Correction for the Wavelength Modulation Characteristics of DFB Lasers, IEEE Photonics J., Vol 8, 3, 2016

BOLSHOV, M., KURITSYN, Y., and ROMANOVSKII, Y., (2015), Tunable diode laser spectroscopy as a technique for combustion diagnostics, Spectrochimica Acta Part B: Atomic Spectroscopy, Vol 106, p45-66, 2015

CHIGHINE, A., FISHER, E., TSEKENIS, S-A. and MCCANN, H., (2015), TDLAS using FPGA-based Lock-In Detection for Multi-Channel Chemical Species Tomography, IEEE Sensors Conference, North Korea, Nov. 2015

FISHER, E., YANG, Y., OUYPORNKOCHAGOM, T., CHIGHINE, A., TSEKENIS, S-A., POLYDORIDES, N., JIA, J., KLIMENTS, J., WRIGHT, P., WILCON, D., LENGDEN, M., ARCHILLA, V., JOHNSTONE, W., and MCCANN, H., (2016), Data Acquisition for Multi-Channel CST of Aero-Engine Exhaust Plume Species and Combustion Diagnostics, Proc. 8th WCIPT, Brazil, 2016

FISHER, E. and BENOY, T., (2018), Interleaving and Error Concealment to Mitigate the Impact of Packet Loss in Resource-Constrained TDLAS/WMS Data Acquisition, IEEE Trans. Instrumentation and Measurement (TIM), Vol 67, No 2, February 2018

FISHER, E., TSEKENIS, S-A., YANG, Y., CHIGHINE, A., POLYDORIDES, N., MCCANN, H., WRIGHT, P., OZANYAN, K., WILSON, D., LENGDEN, M. and JOHNSTONE, W., (2018), An Embedded Processing Design for 192-Channel 10-40 MS/s Aero-Engine Optical Tomography, Proc. IEEE International Instrumentation and Measurement Technology Conference (I2MTC), May 2018, Houston Texas, USA

HARLEY, J., ROLLING, A., WISNIEWSKI, C. and GROSS, K., (2012), Spatially Resolved Infrared Spectra of F109 Turbofan Exhaust, Proc. SPIE Vol 8354, Thermosense: Thermal Infrared Applications, 2012

LASCOS, S. and CASSIDY, D., (2008), Multichannel Digital Phase Sensitive Detection using a Field Programmable Gate Array Development Platform, Review of Scientific Instruments, Vol 79, 074702, 2008

MA, L., XUESONG, L., SANDERS, S., CASWELL, A., ROY, S., PLEMMONS, D. and GORD, J., (2013), 50-kHz-rate 2D Imaging of Temperature and H2O Concentration at the Exhaust Plane of a J85 Engine using Hyperspectral Tomography, Optics Express, OSA, Vol 21, No 1, 2013

POLYDORIDES, N., TSEKENIS, S-A., FISHER, E., CHIGHINE, A., MCCANN, H., DIMICCOLI, L, WRIGHT, P, LENGDEN, M., BENOY, T., WILSON, D., HUMPHRIES, G. and JOHNSTONE, W., (2018), A Constrained Solver for Optical Absorption Tomography, Applied Optics, Vol 57, 7, 2018

RIEKER, G., JEFFRIES, J. and HANSON, R, (2009), Calibration-free wavelength modulation spectroscopy for measurement of gas temperature and concentration in harsh environments, Applied Optics, Vol 48, 29, 2009

TSEKENIS, S-A., POLYDORIDES, N., FISHER, E., CHIGHINE, A., JIA, J., MCCANN, H., WILSON, D., HUMPHRIES, G, LENGDEN, M., BENOY, T., JOHNSTONE, W., KILMENTS, J., WRIGHT, P., FENG, Y., NILSSON, J. and ARCHILLA, V., (2016), Chemical Species Tomography of Carbon Dioxide, Proc. 8th WCIPT, Brazil, 2016

WILSON, D., ARMSTRONG, I., LENGDEN, M. and JOHNSTONE, W., (2014), In-situ Measurement of Combustion Produced CO2 in the 2 μm Region, within a Jet Engine Exhaust Plume, Proc. Field Laser Applications in Industry and Research (FLAIR), May 2014, Italy.

WRIGHT, P., MCCORMICK, D., KILMENTS, J., OZANYAN, K, TSEKENIS, S-A., FISHER, E., MCCANN, H., ARCHILLA, V., GONZALEZ-NUNEZ, A, JOHNSON, M., BLACK, J., LENGDEN, M., WILSON, D., JOHNSTONE, W., FENG, Y. and NILSSON, J, (2016), Implementation of Non-Intrusive Jet Exhaust Species Distribution Measurements Within a Test Facility, Proc IEEE Aerospace Conference, Montana, USA, 5-12 March 2016

XILINX, XAPP524 – Serial LVDS High-Speed ADC Interface – Defossez, M, Application Note 7 Series FPGSs, November 2012, Accessed 2nd June 2018, URL: https://www.xilinx.com/support/documentation/application_notes/xapp524-serial-lvds-adc-interface.pdf